In response to the office action in this case mailed September 4, 2003, the Applicant's attorney, Bryan Santarelli, request that the application be amended as follows.

In the Drawings:

Please amend the drawings as requested in the enclosed request for drawing change.

In the Specification:

Please replace the paragraphs beginning at Column 1, line 6 and ending at Column 2, line 6 with the following:

The subject matter of the present application is related to [copending U.S. application Ser. No. 08/173,197, filed Dec. 22, 1993] U.S. Pat. No. 5,577,051, titled "Improved Static Memory Long Write Test", [attorney docket no. 93-C-82, copending U.S. application Ser. No. 08/172,854, filed Dec. 22, 1993] U.S. Pat. No. 5,835,427, titled "Stress Test Mode", [attorney docket no. 93-C-56] all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following [pending U.S. patent applications] U.S. patents by David Charles McClure entitled:

"Architecture Redundancy", [Ser. No. 08/582,484 (Attorney's Docket No. 95-C-136)] U.S. Pat. No. 5,612,918, and

"[(]Redundancy Control", [Ser. No. 08/580,827 (Attorney's Docket No. 95-C-143)] U.S. Pat. No. 5,790,462, which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are [arguable] arguably related to the present application, which are herein incorporated by reference;
and entitled:

"Test Mode Activation and Data Override", Ser. No. 08/587,709 [Attorney's Docket No. 95-C-137)],

"Pipelined Chip Enable Control Circuitry and Methodology", [Ser. No. 08/588,730_(Docket No. 95-C-138)] U.S. Pat. No. 5,701,275,

"Output Driver Circuitry Having a Single Slew Rate Resistor", [Ser. No. 08/588,988 (Docket No. 95-C-139)] U.S. Pat. No. 5,801,563,

"Synchronized Stress Test Control", [Ser. No. 08/589,015 (Docket No. 95-C-142)] U.S. Pat. No. 5,712,584,

"Write Pass Through Circuit", [Ser. No. 08/588,662 (Attorney's Docket No. 95-C-144)] U.S. Pat. No. 5,657,292,

"Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", [Ser. No. 08/588,762 (Attorney's Docket No. 95-C-145)] U.S. Pat. No. 5,845,059,

"Synchronous Output Circuit", [Ser. No. 08/588,901 (Attorney's Docket No. 95-C-146)] U.S. Pat. No. 5,619,456,

"Write Driver Having a Test Function", [Ser. No. 08/589,141 (Attorney's Docket No. 95-C-147)] U.S. Pat. No. 5,745,432,

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 [(Attorney's Docket No. 95-C-148)] (since abandoned),

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 [(Attorney's Docket No. 95-C-149)] (since abandoned),

"Clocked Sense Amplifier with Wordline Tracking", [Ser. No. 08/587,728 (Attorney's Docket No. 95-C-150)] U.S. Pat. No. 5,802,004,

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 [(Attorney's Docket No. 95-C-151)] (since abandoned),

"Device and Method for Isolating Bit Lines from a Data Line", [Ser. No. 08/588,740 (Attorney's Docket No. 95-C-154)] U.S. Pat. No. 5,691,950,

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", [Ser. No. 08/587,711 (Attorney's Docket No. 95-C-156)] U.S. Pat. No. 5,864,696,

"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", [Ser. No. 08/589,024,] U.S. Pat. No. 5,619,466 [(Attorney's Docket No. 95-C-168],

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 [(Attorney's Docket No. 169] (since abandoned),

and the following [pending U.S. patent applications] U.S. patents by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 [(Attorney's Docket No. 95-C-141)] (since abandoned),

"Switching Master/Slave Circuit", [Ser. No. 08/588,648 (Attorney's Docket No. 96-C-03) U.S. Pat. No. 5,783,958, which have the same effective filing data and ownership